FIGURE 1

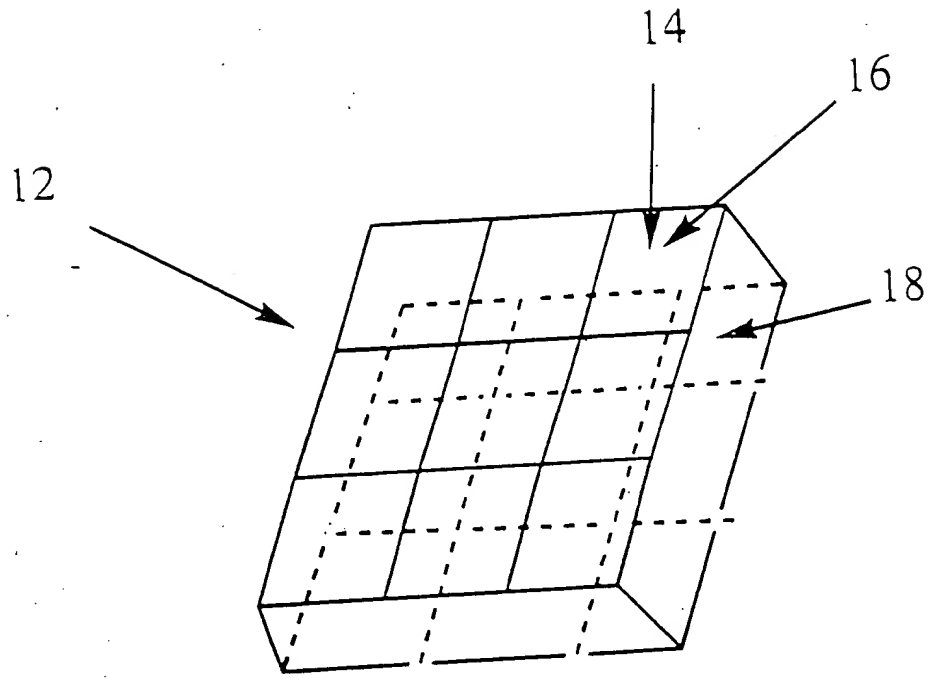


FIGURE 2

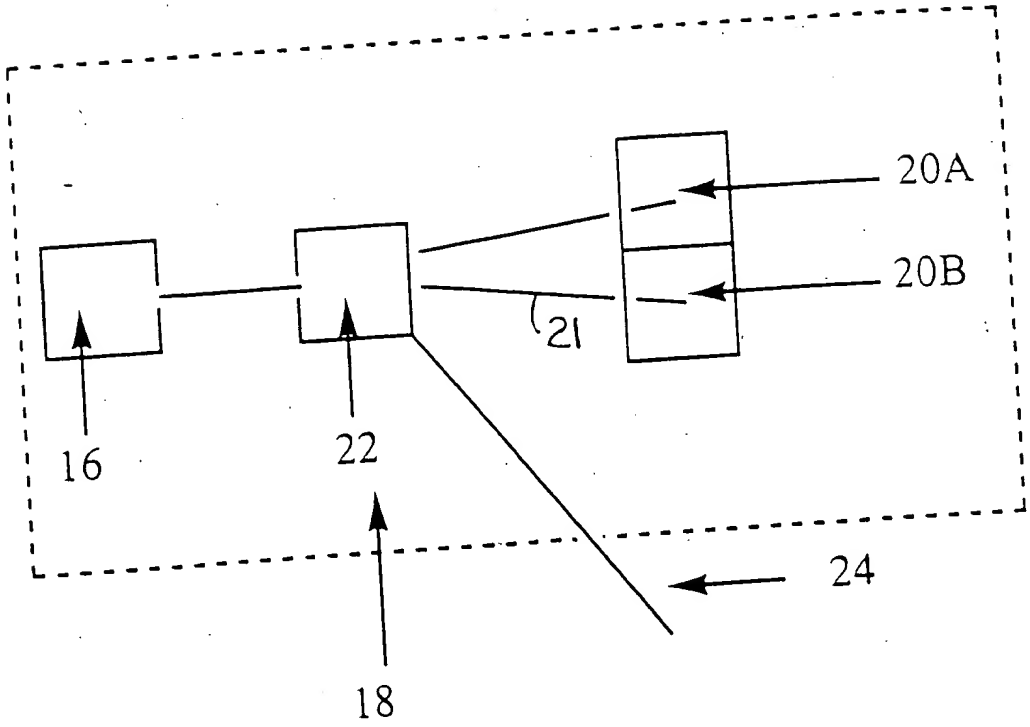


FIGURE 3

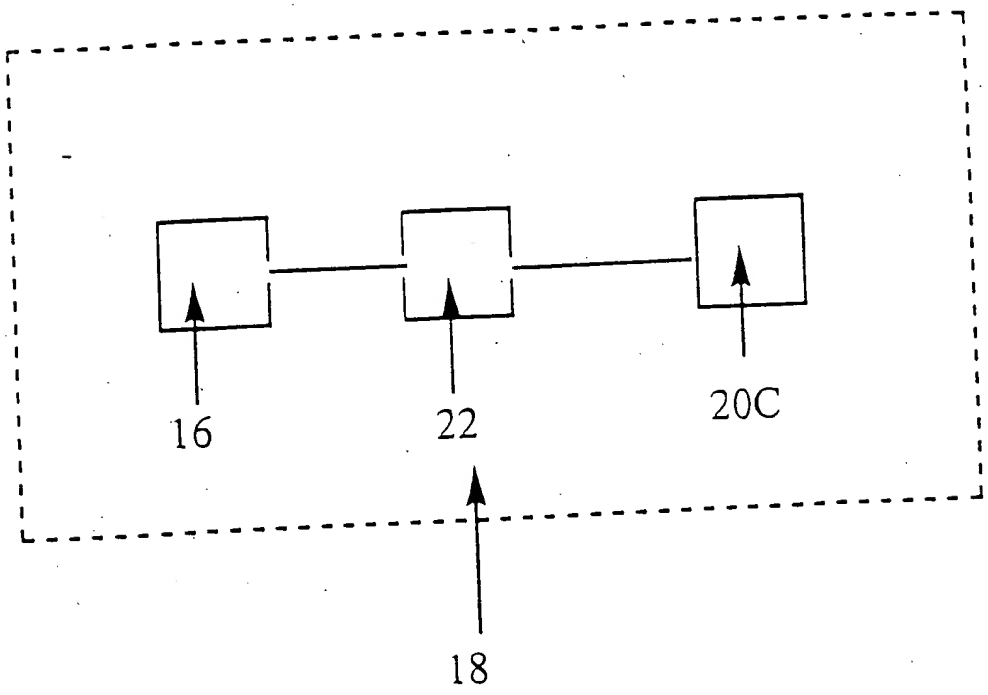


FIGURE 4A

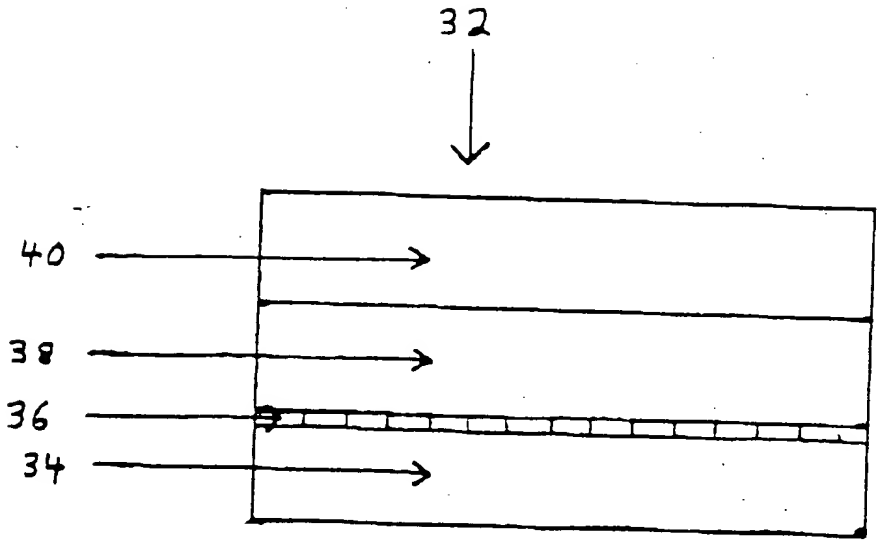


FIGURE 4B

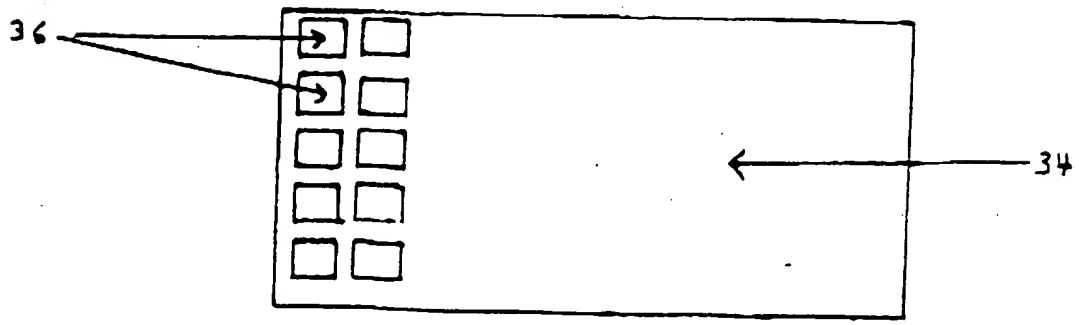


FIGURE 5

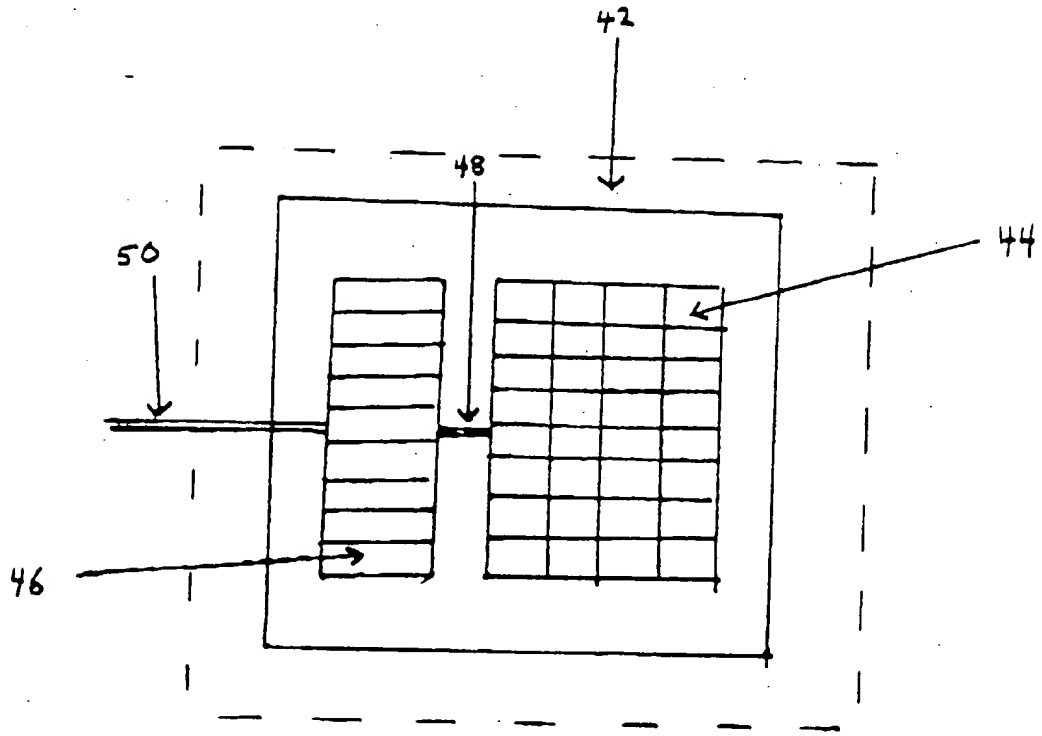


FIGURE 6

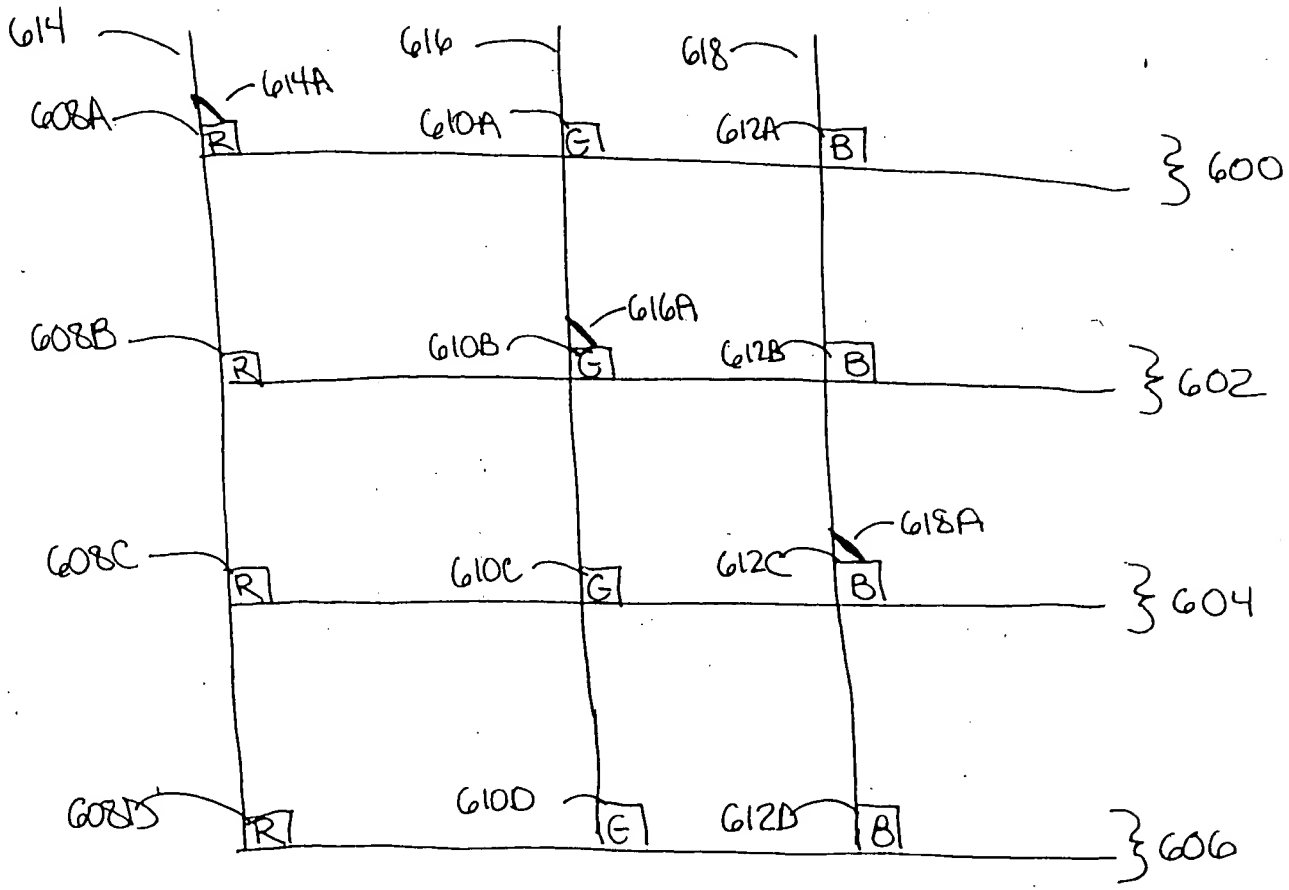

614
616
618
614A
608A
610A
612A
R
G
B
600
608B
616A
610B
612B
602
608C
618A
610C
612C
604
608D
610D
612D
606

FIGURE 7A

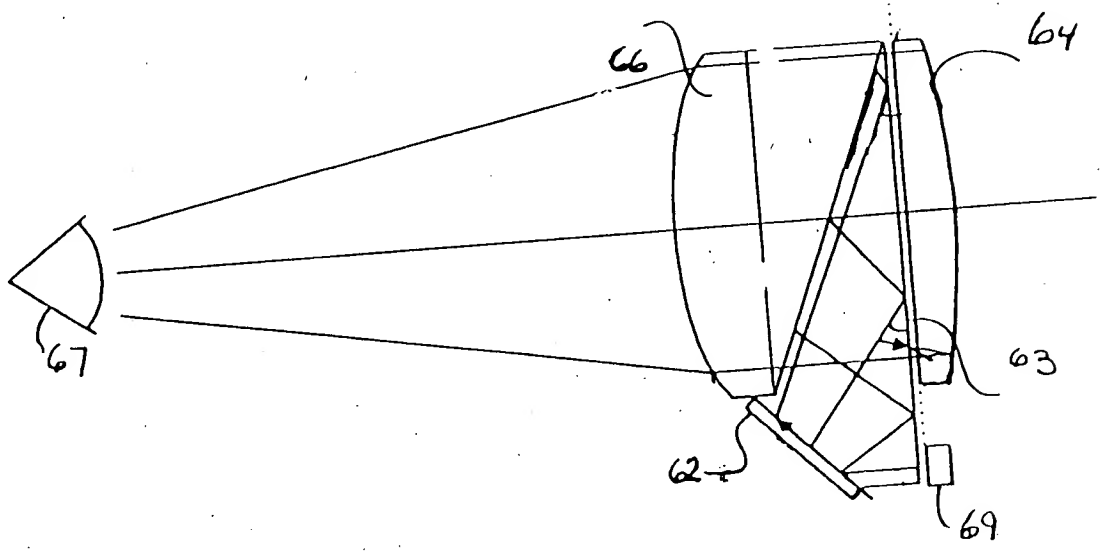


FIGURE 7B

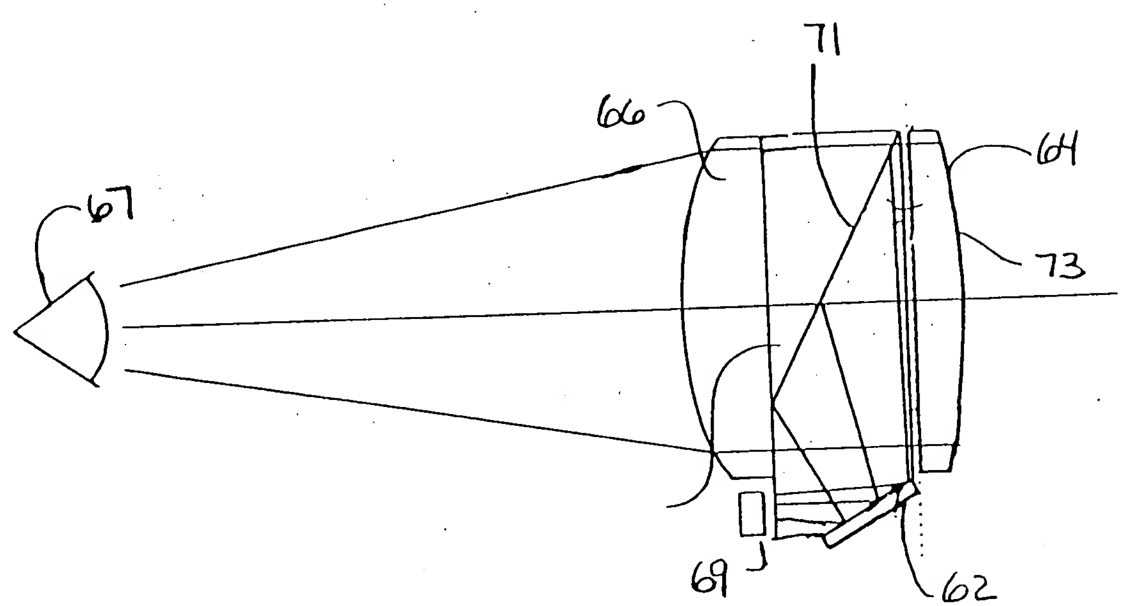


FIGURE 7C

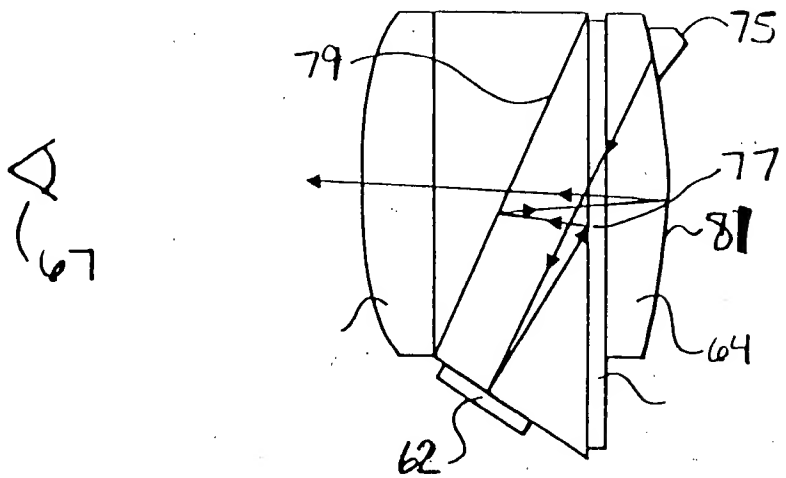


FIGURE 8A

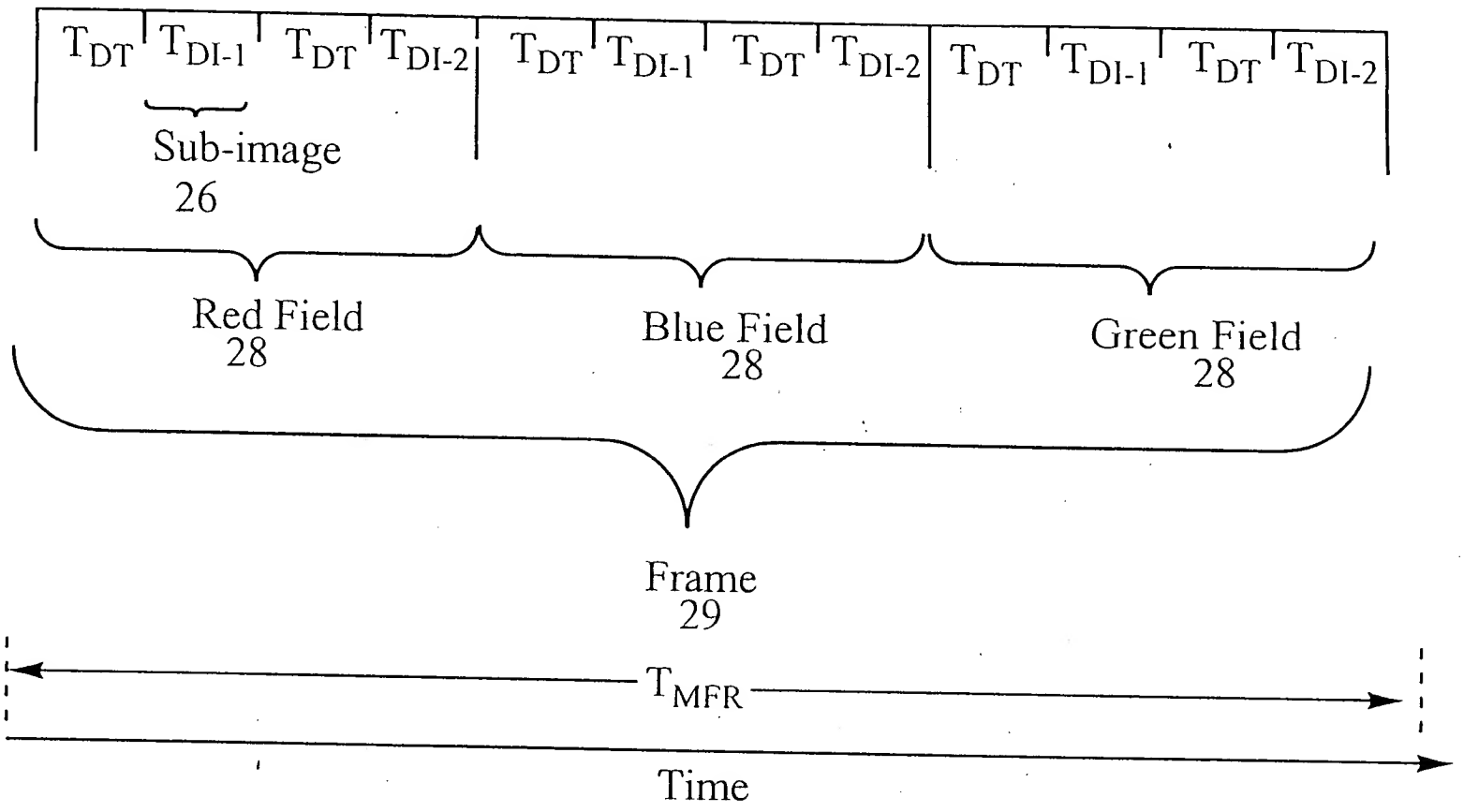

T_{DT} T_{DI-1} T_{DT} T_{DI-2} T_{DT} T_{DI-1} T_{DT} T_{DI-2} T_{DT} T_{DI-1} T_{DT} T_{DI-2}
Sub-image
26
Red Field
28
Blue Field
28
Green Field
28
Frame
29
T_{MFR}
Time

FIGURE 8B

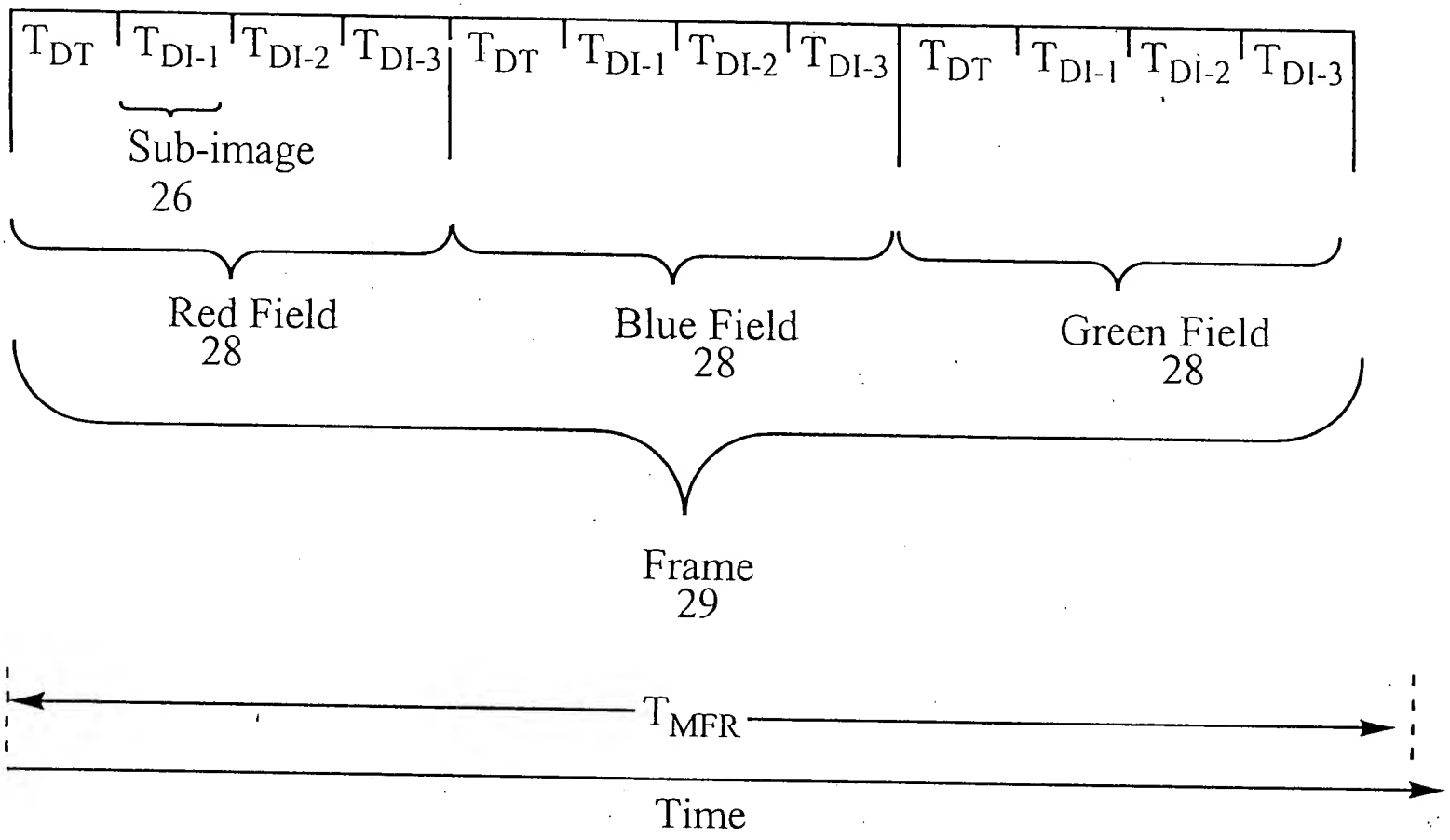

T_{DT} T_{DI-1} T_{DI-2} T_{DI-3} T_{DT} T_{DI-1} T_{DI-2} T_{DI-3} T_{DT} T_{DI-1} T_{DI-2} T_{DI-3}
Sub-image
26
Red Field
28
Blue Field
28
Green Field
28
Frame
29
T_{MFR}
Time

FIGURE 8C

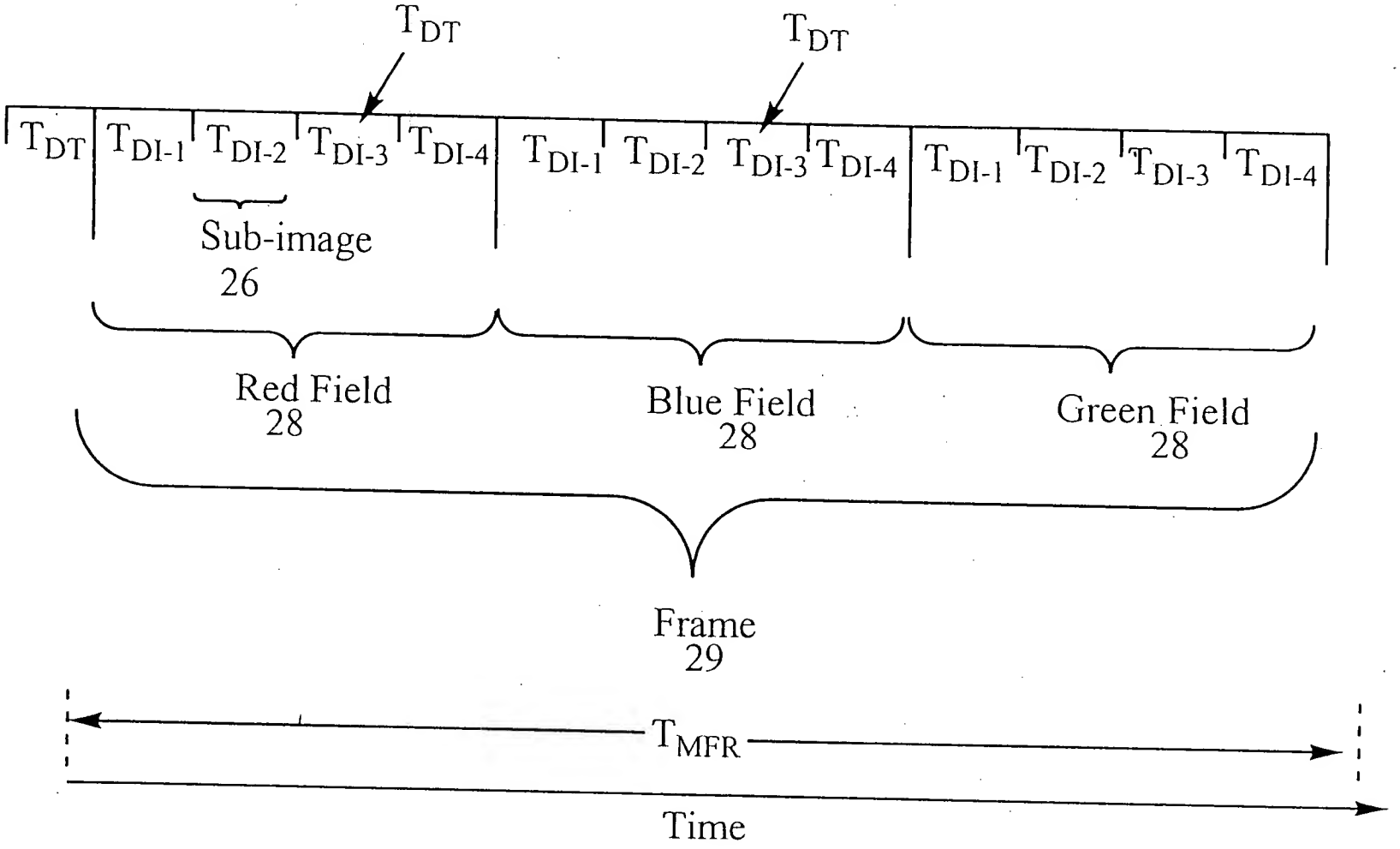

T_{DT}
T_{DT}
T_{DT} T_{DI-1} T_{DI-2} T_{DI-3} T_{DI-4} T_{DI-1} T_{DI-2} T_{DI-3} T_{DI-4} T_{DI-1} T_{DI-2} T_{DI-3} T_{DI-4}
Sub-image
26
Red Field
28
Blue Field
28
Green Field
28
Frame
29
T_{MFR}
Time

FIGURE 9A

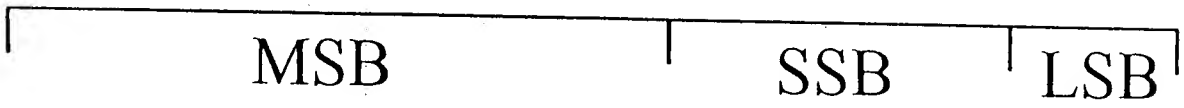


FIGURE 9B

MSB most significant bit
SSB second significant bit
LSB least significant bit

FIGURE 10

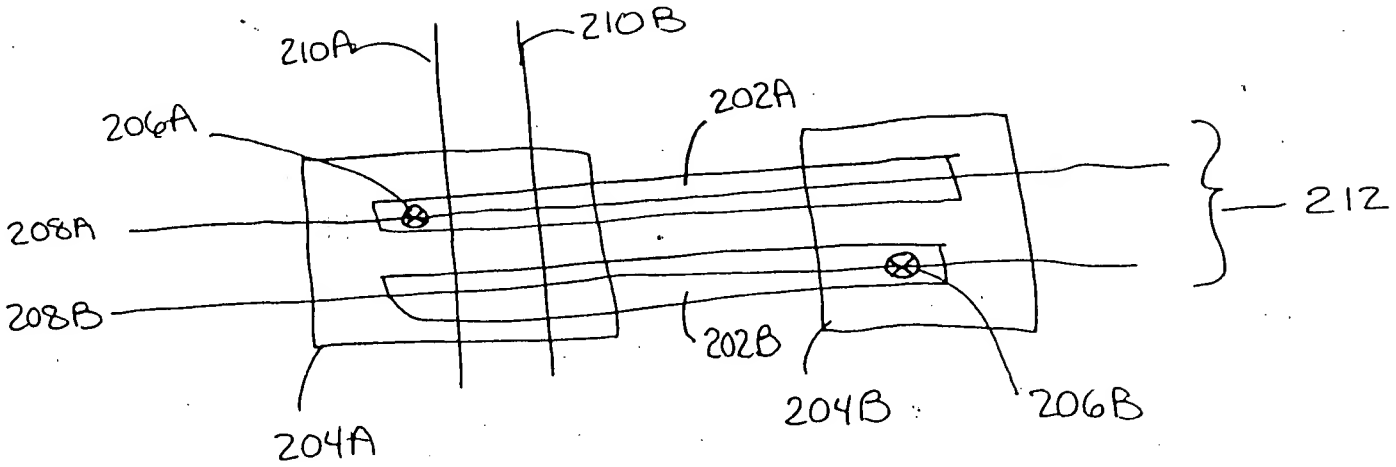


FIGURE 11

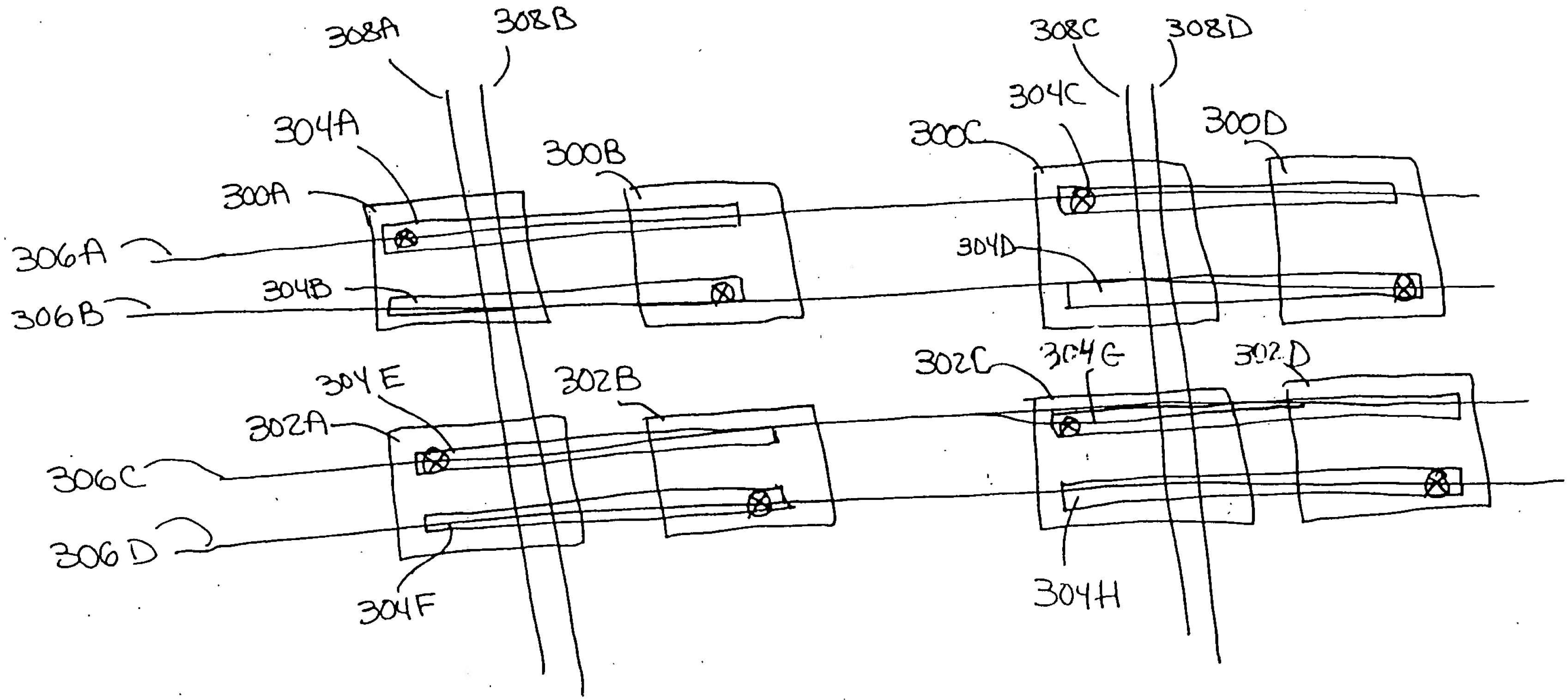


FIGURE 12

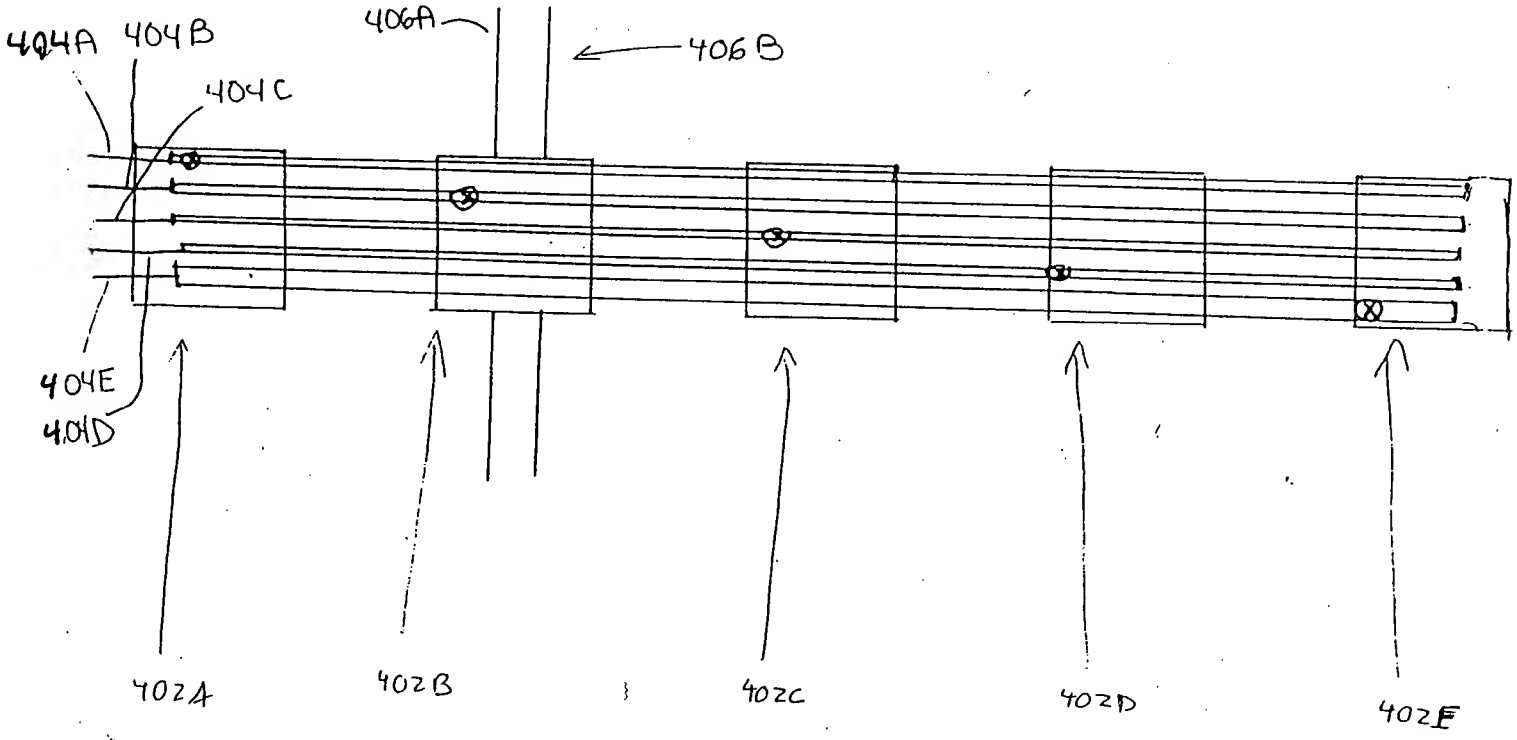


FIGURE 13

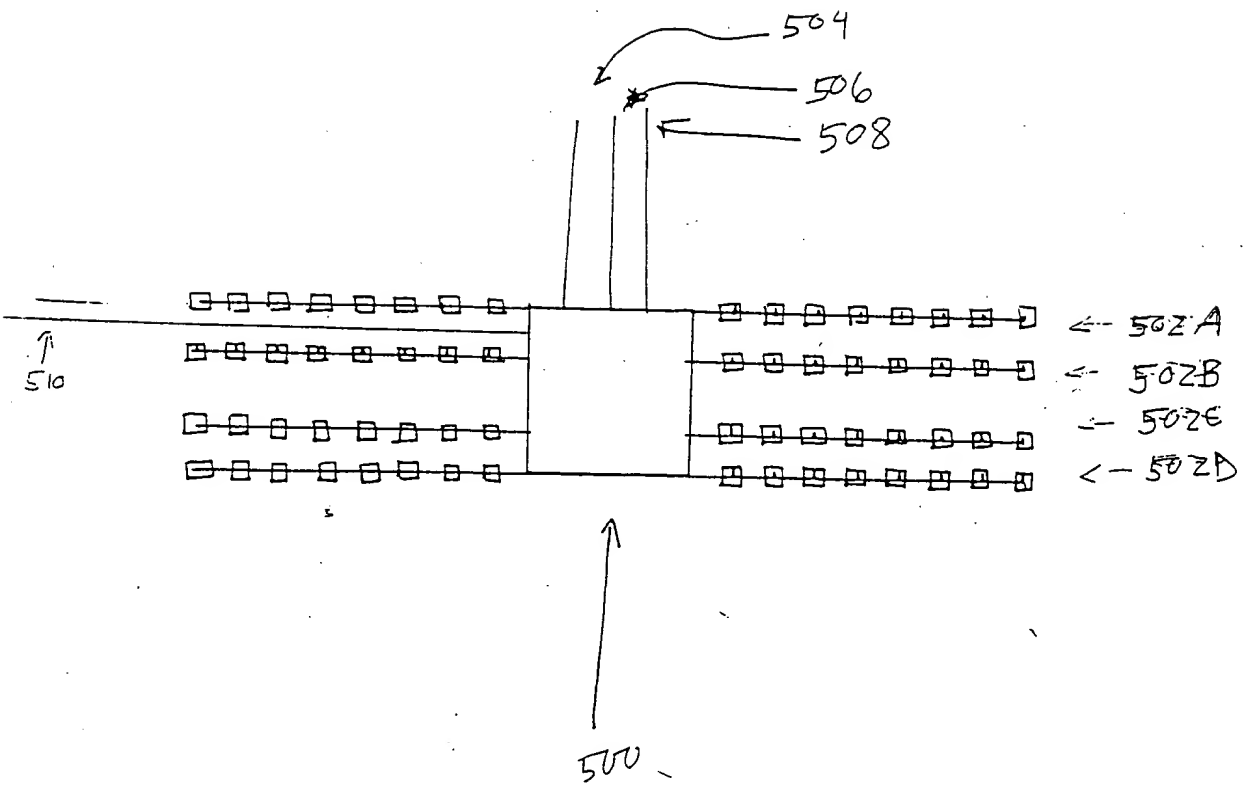


FIGURE 14

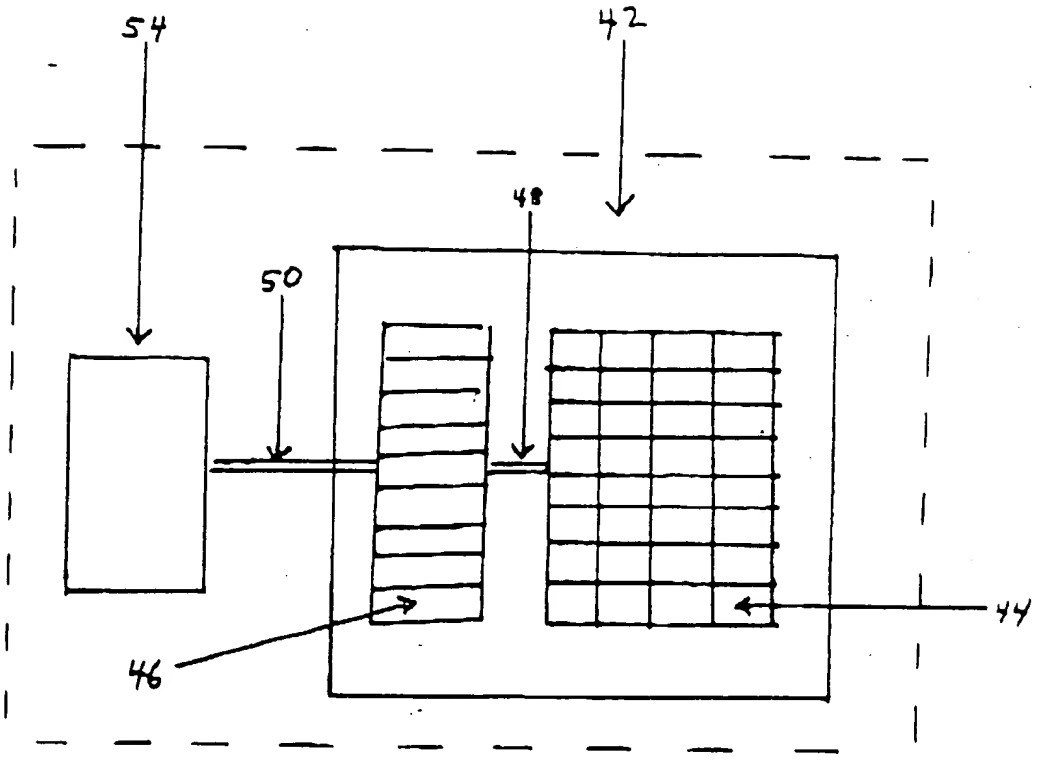
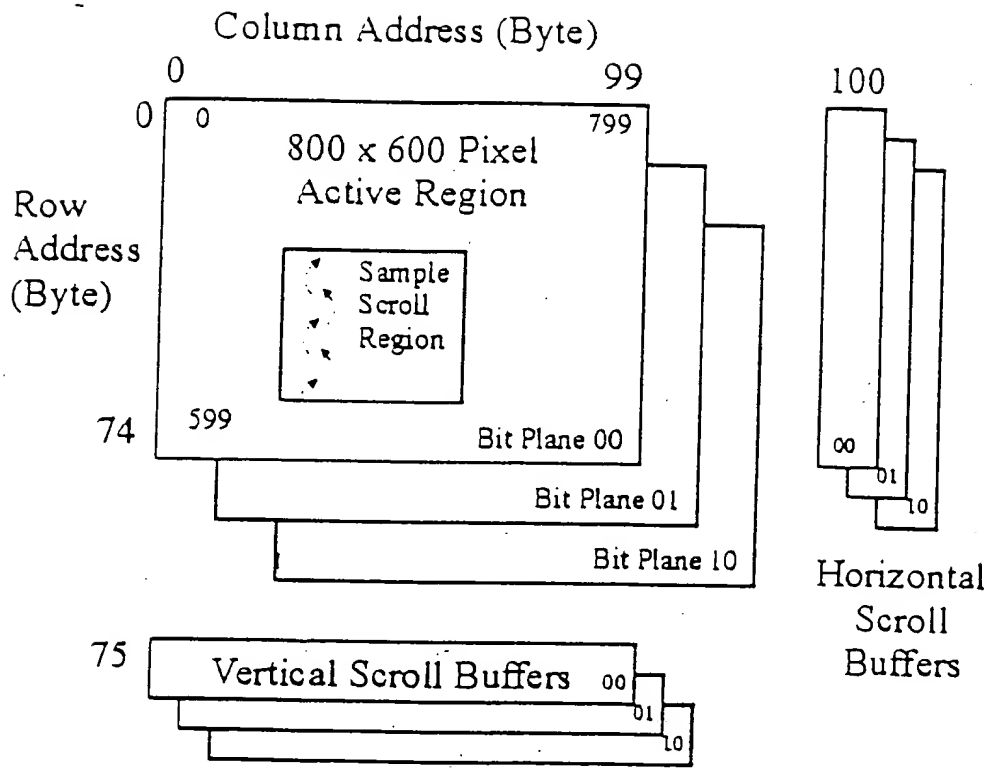
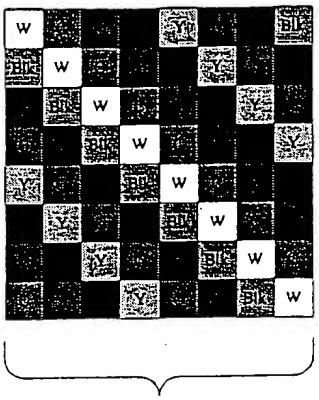


FIGURE 15A

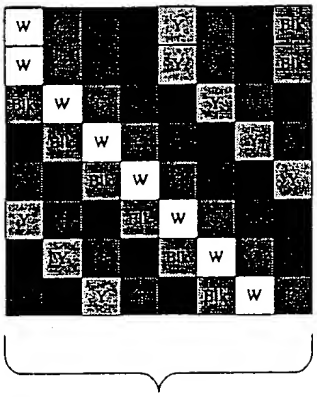

Column Address (Byte)
0
99
100
0
0
799
800 x 600 Pixel
Active Region
Row
Address
(Byte)
Sample
Scroll
Region
74
599
Bit Plane 00
Bit Plane 01
Bit Plane 10
00
01
10
Horizontal
Scroll
Buffers
75
Vertical Scroll Buffers
00
01
10



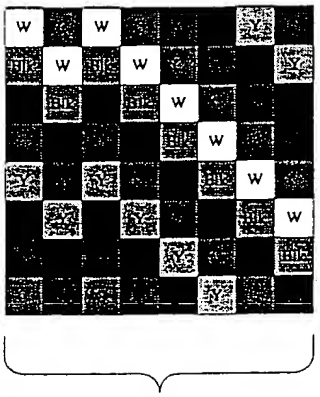
Original Scroll Region

Key

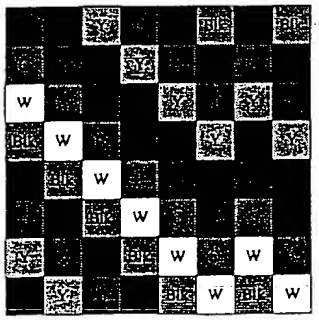
B	G	R	Color	Pixel
0	0	0	White	
0	0	1	Cyan	
0	1	0	Magenta	
0	1	1	Blue	
1	0	0	Yellow	
1	0	1	Green	
1	1	0	Red	
1	1	1	Black	



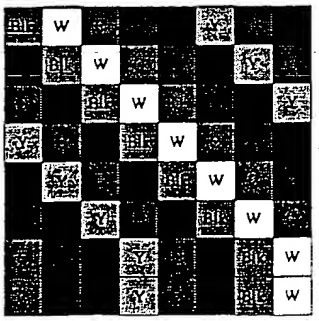
Scroll Up



Scroll Left



Scroll Right



Scroll Down

FIGURE 15B

FIGURE 16

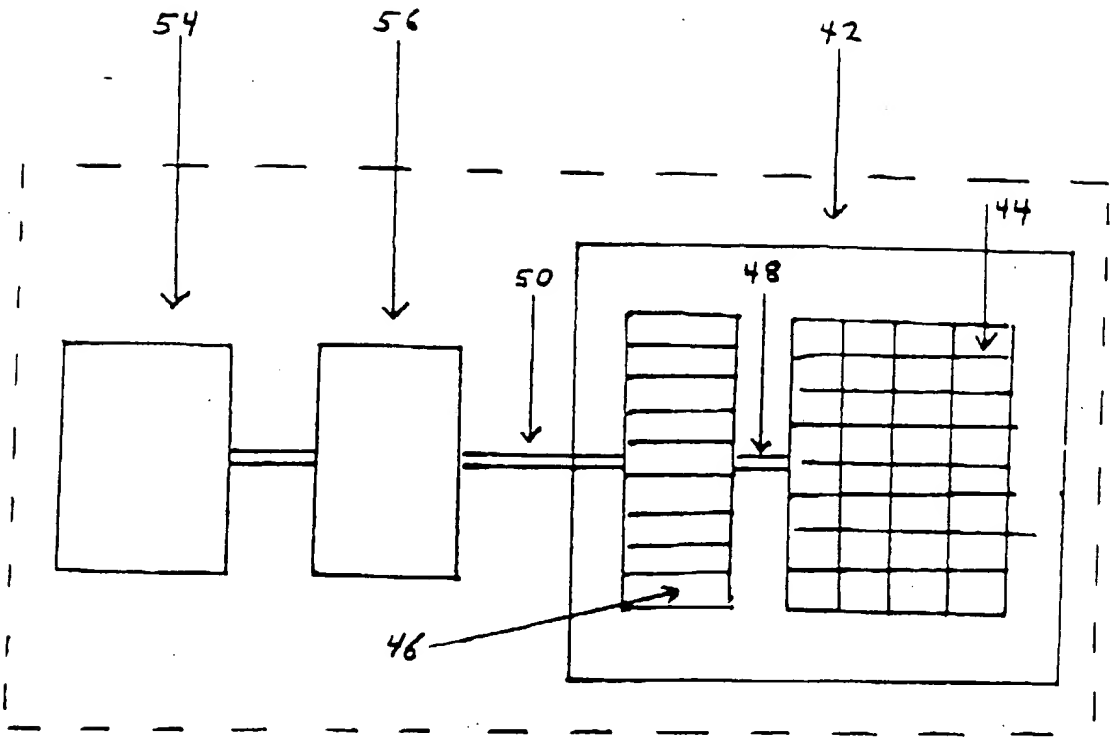


FIGURE 17

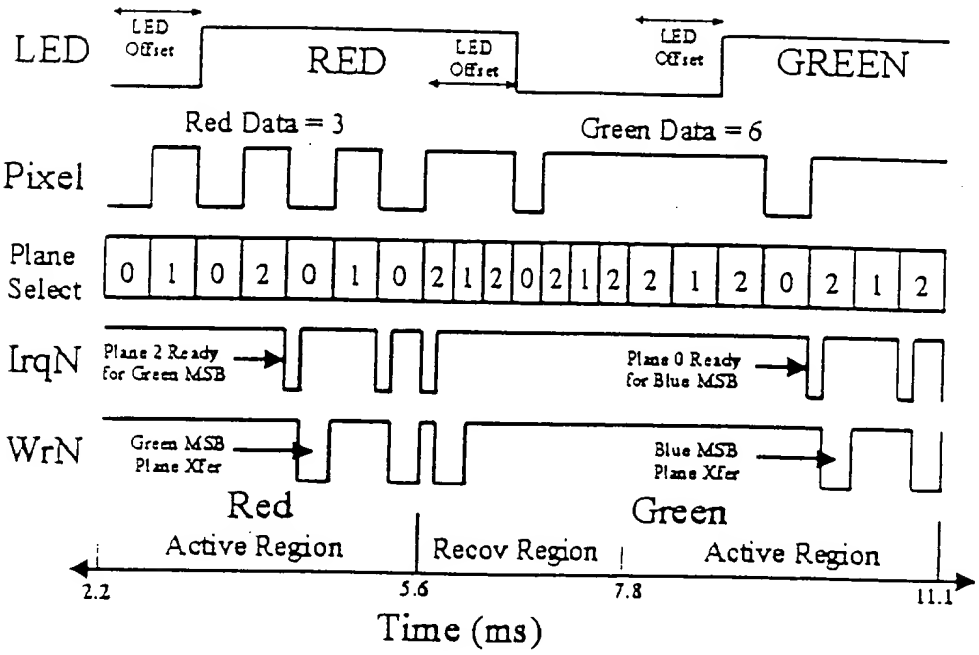
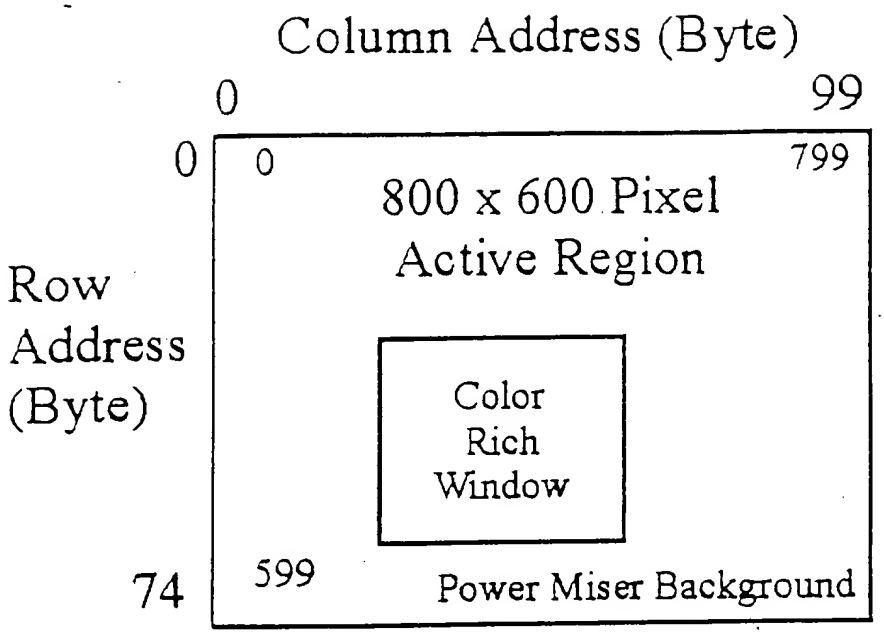

LED
LED Offset
RED
LED Offset
LED Offset
GREEN
Red Data = 3
Green Data = 6
Pixel
Plane Select
0 1 0 2 0 1 0 2 1 2 0 2 1 2 2 1 2 0 2 1 2
IrqN
Plane 2 Ready for Green MSB
Plane 0 Ready for Blue MSB
WrN
Green MSB Plane Xfer
Blue MSB Plane Xfer
Red
Active Region
Recov Region
Green
Active Region
2.2
5.6
7.8
11.1
Time (ms)

FIGURE 18


Column Address (Byte)
0
99
0
0
799
800 x 600 Pixel
Active Region
Row
Address
(Byte)
Color
Rich
Window
74
599
Power Miser Background

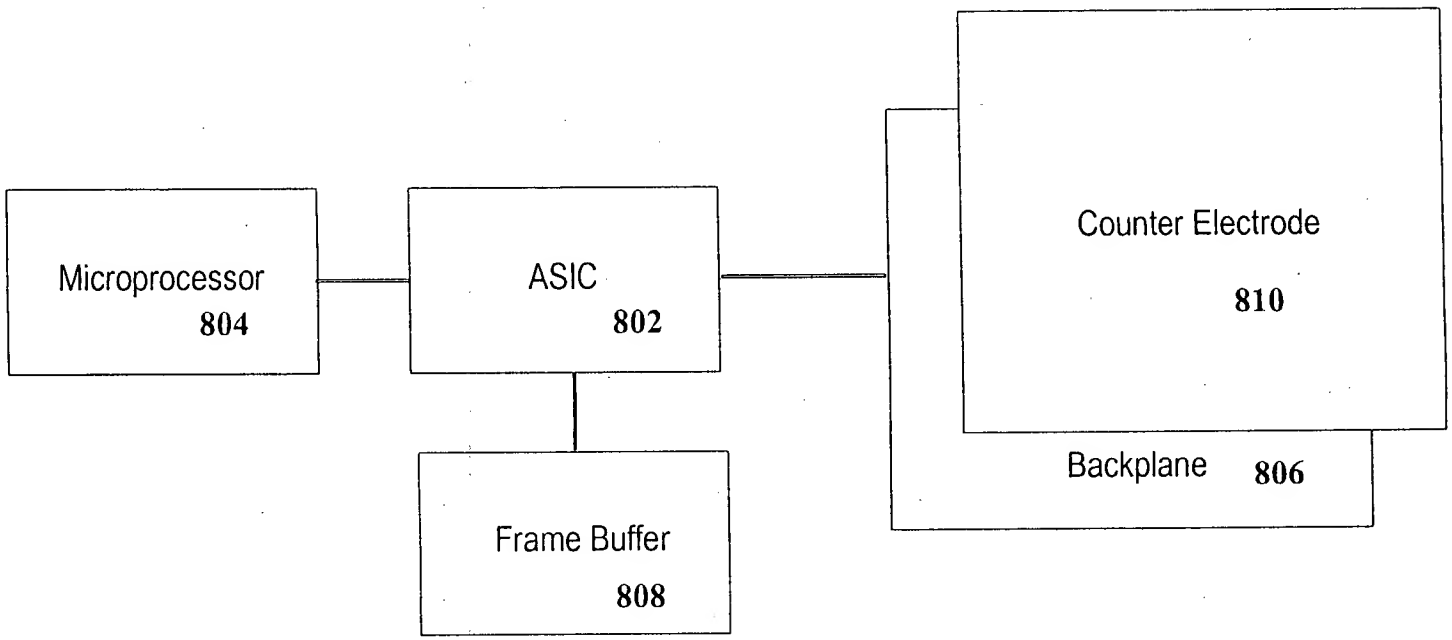

Microprocessor
804
ASIC
802
Frame Buffer
808
Counter Electrode
810
Backplane
806

Fig. 19

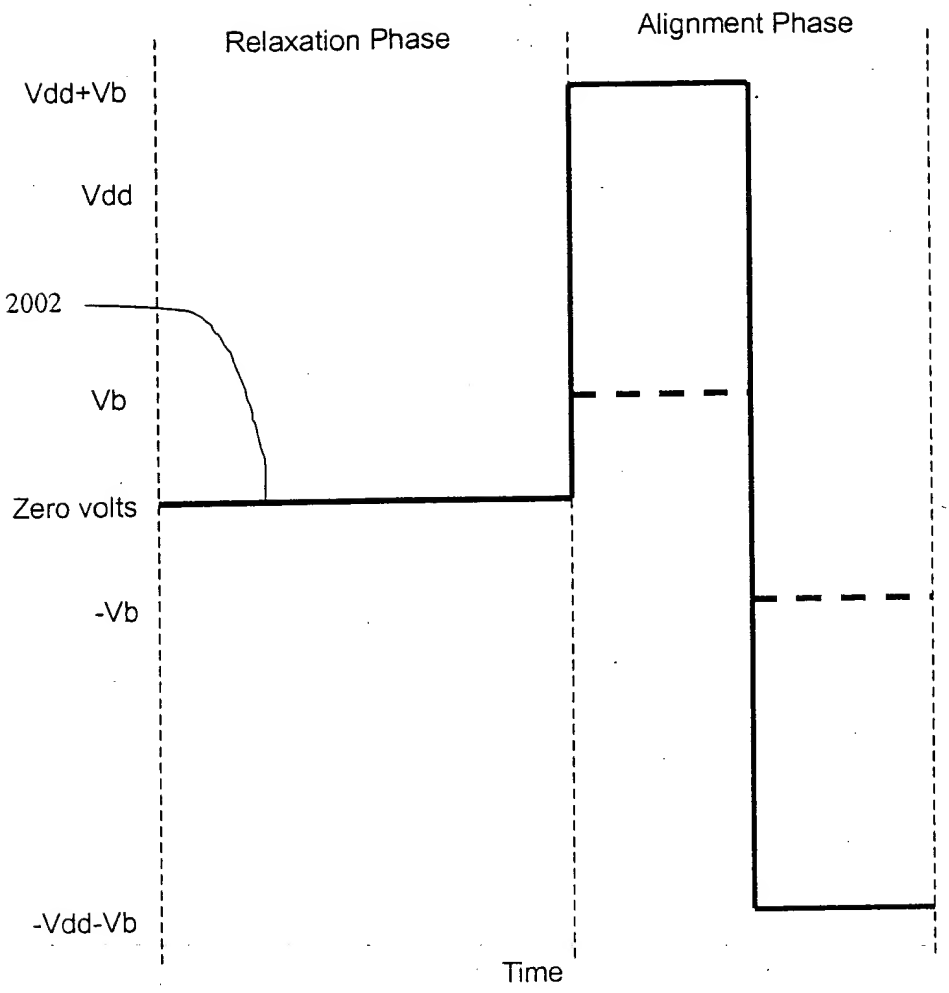

Relaxation Phase
Alignment Phase
Vdd+Vb
Vdd
2002
Vb
Zero volts
-Vb
-Vdd-Vb
Time

Fig. 20

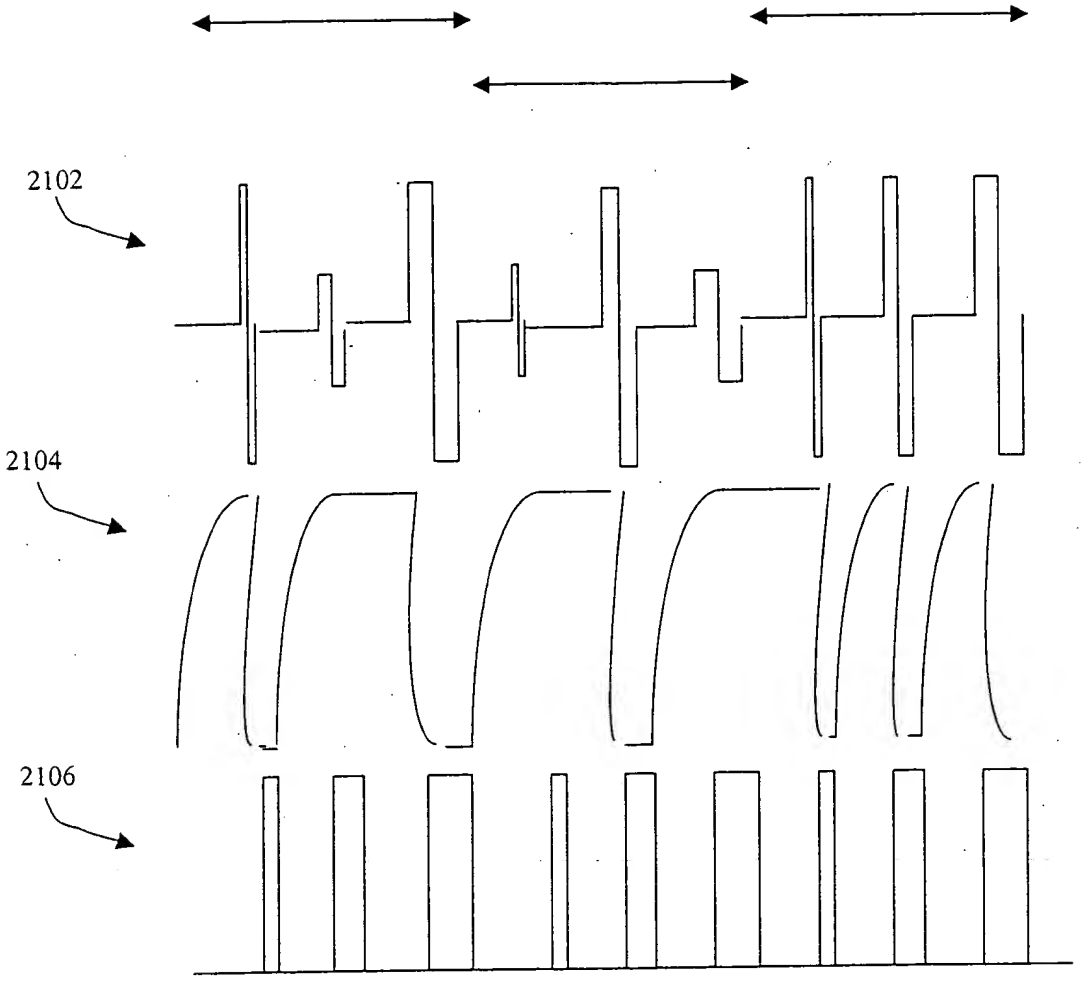


Fig. 21

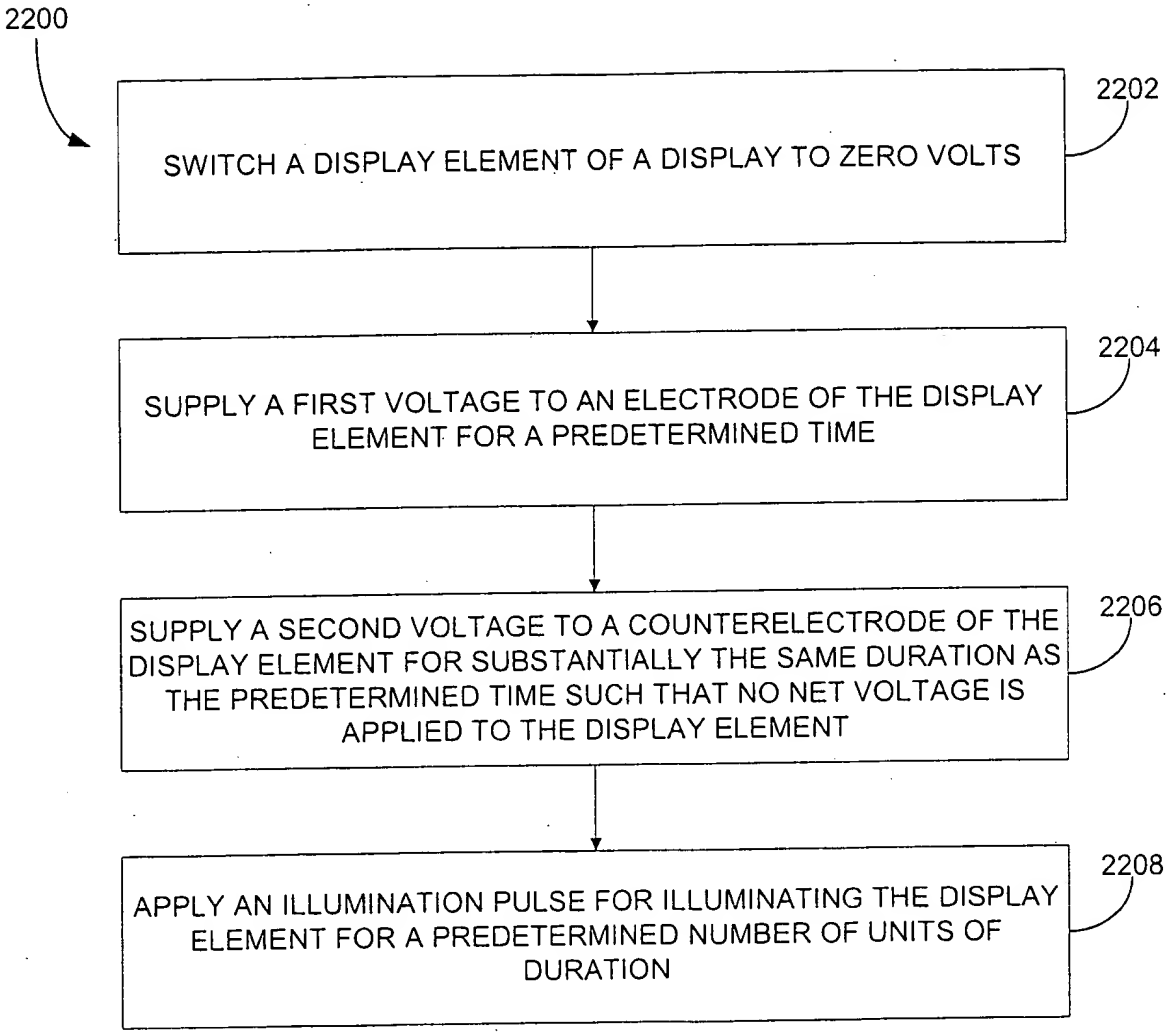

2200
SWITCH A DISPLAY ELEMENT OF A DISPLAY TO ZERO VOLTS
2202
SUPPLY A FIRST VOLTAGE TO AN ELECTRODE OF THE DISPLAY ELEMENT FOR A PREDETERMINED TIME
2204
SUPPLY A SECOND VOLTAGE TO A COUNTERELECTRODE OF THE DISPLAY ELEMENT FOR SUBSTANTIALLY THE SAME DURATION AS THE PREDETERMINED TIME SUCH THAT NO NET VOLTAGE IS APPLIED TO THE DISPLAY ELEMENT
2206
APPLY AN ILLUMINATION PULSE FOR ILLUMINATING THE DISPLAY ELEMENT FOR A PREDETERMINED NUMBER OF UNITS OF DURATION
2208

Fig. 22

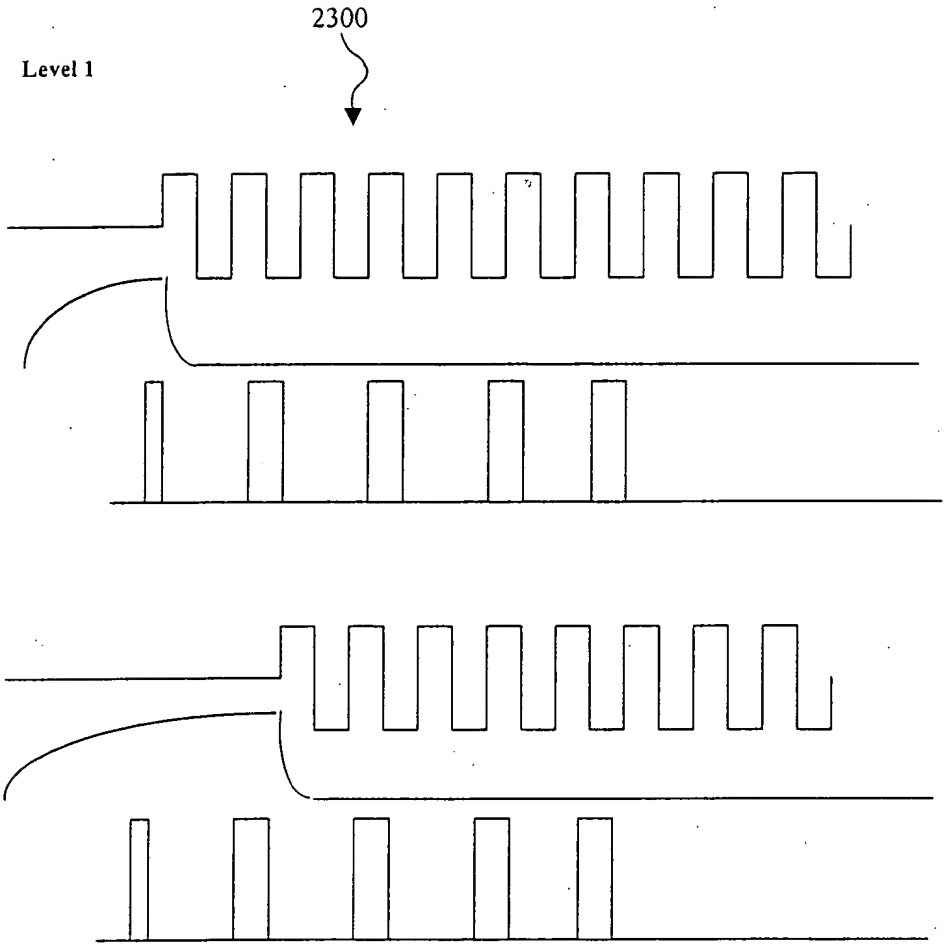


Fig. 23

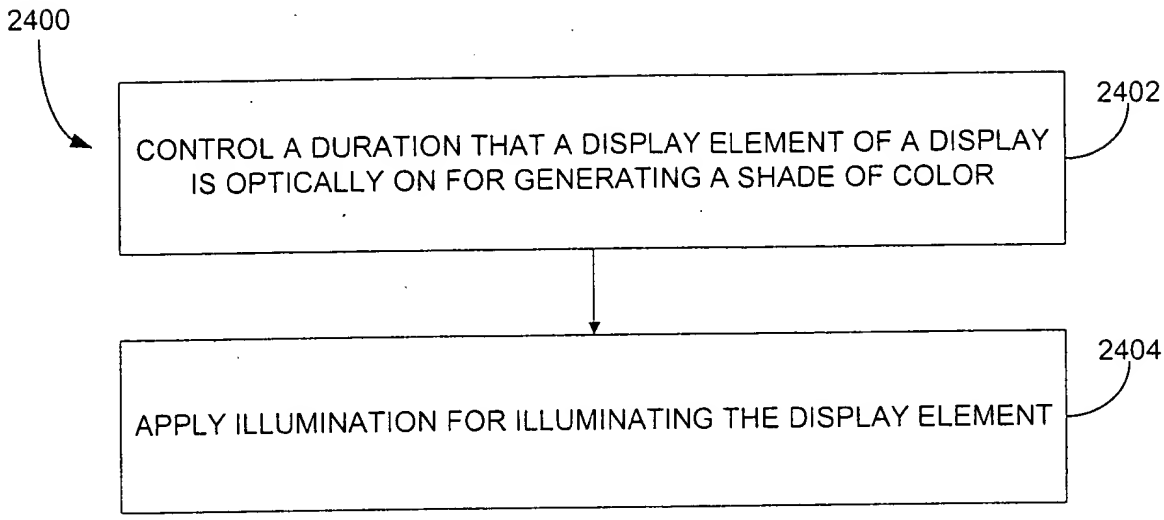

2400
CONTROL A DURATION THAT A DISPLAY ELEMENT OF A DISPLAY IS OPTICALLY ON FOR GENERATING A SHADE OF COLOR
2402
APPLY ILLUMINATION FOR ILLUMINATING THE DISPLAY ELEMENT
2404

Fig. 24

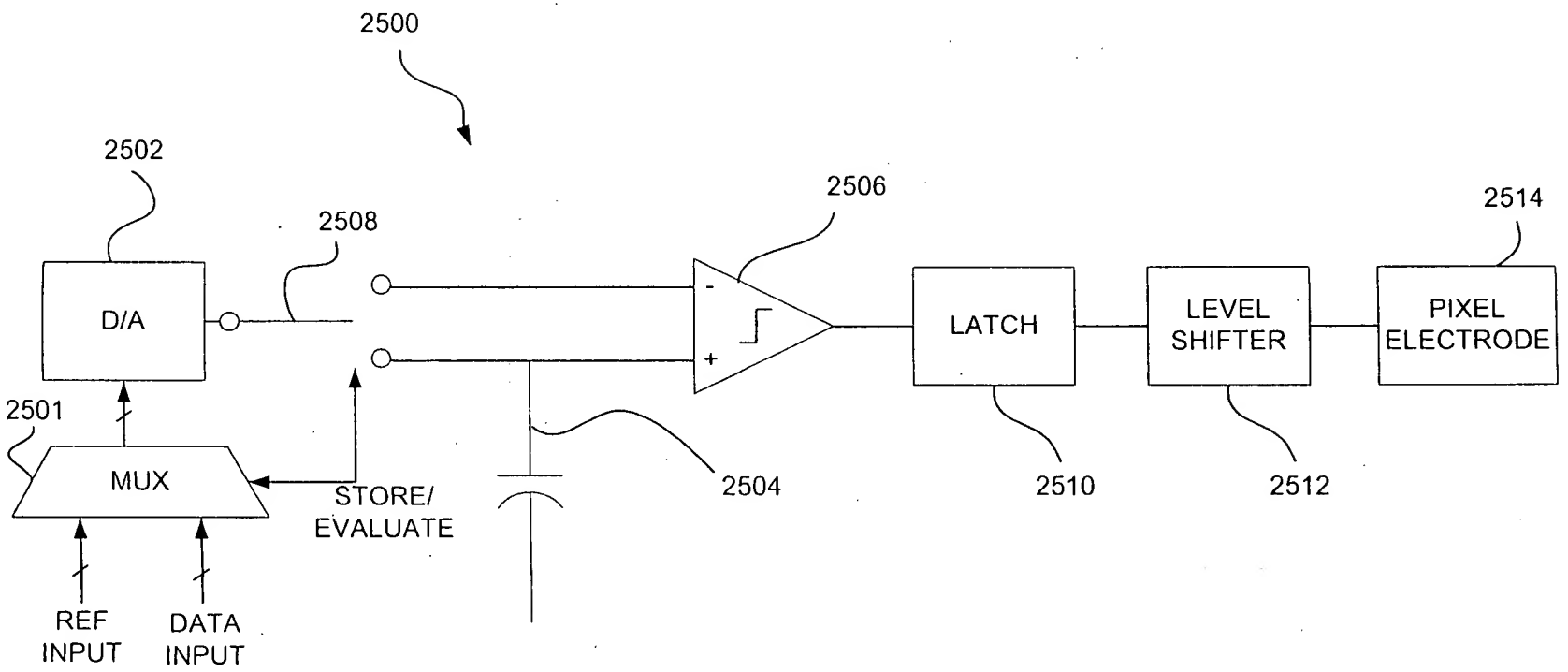


Fig. 25A

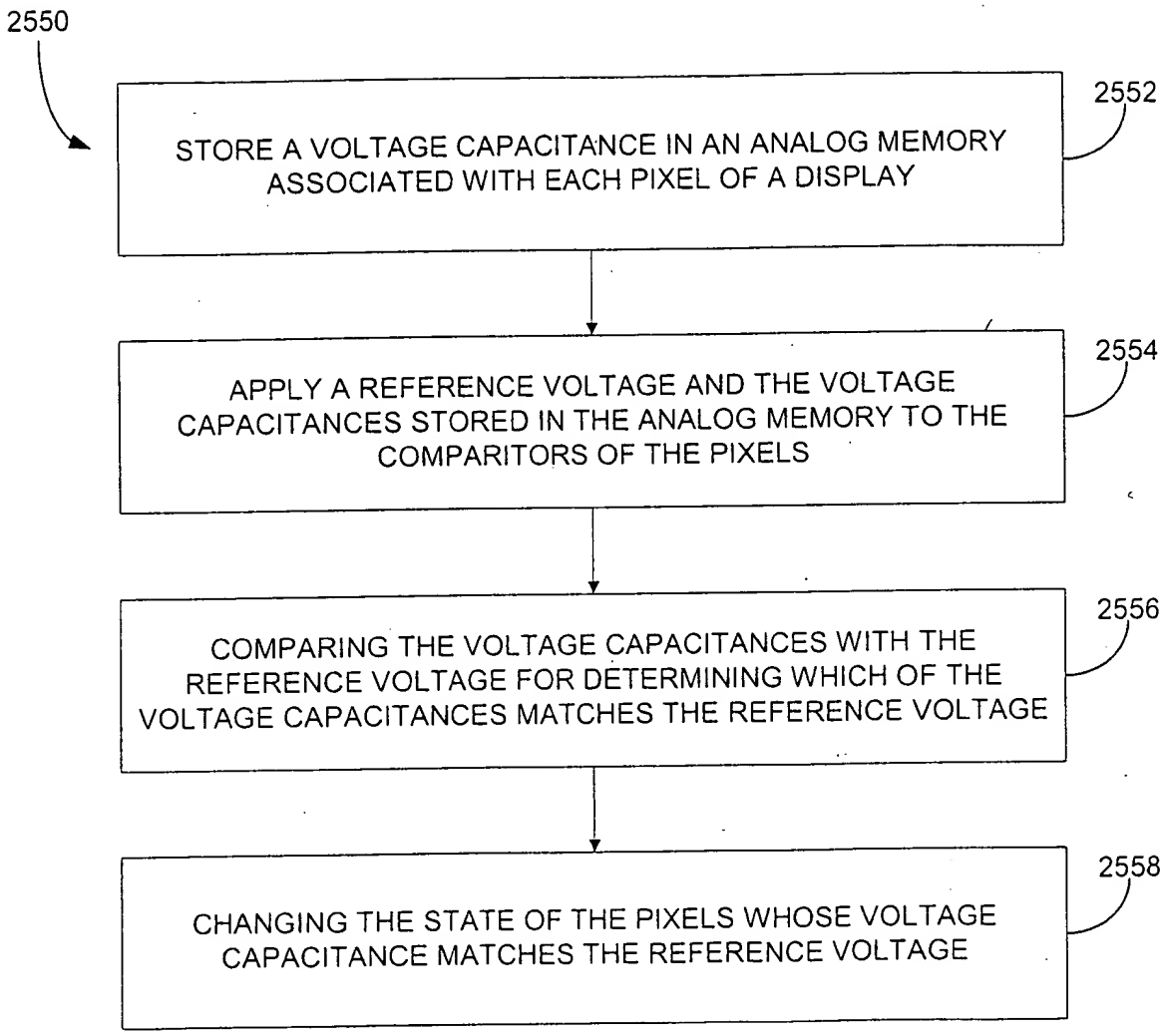

2550
STORE A VOLTAGE CAPACITANCE IN AN ANALOG MEMORY ASSOCIATED WITH EACH PIXEL OF A DISPLAY
2552
APPLY A REFERENCE VOLTAGE AND THE VOLTAGE CAPACITANCES STORED IN THE ANALOG MEMORY TO THE COMPARITORS OF THE PIXELS
2554
COMPARING THE VOLTAGE CAPACITANCES WITH THE REFERENCE VOLTAGE FOR DETERMINING WHICH OF THE VOLTAGE CAPACITANCES MATCHES THE REFERENCE VOLTAGE
2556
CHANGING THE STATE OF THE PIXELS WHOSE VOLTAGE CAPACITANCE MATCHES THE REFERENCE VOLTAGE
2558

Fig. 25B

Columns

Rows

A	B	A	B
B	A	B	A
A	B	A	B

Fig. 26

Columns

Rows

A	B	C	D	A	B	C	D
C	D	A	B	C	D	A	B
B	A	D	C	B	A	D	C
D	C	B	A	D	C	B	A
A	B	C	D	A	B	C	D
C	D	A	B	C	D	A	B

Fig. 27